REMARKS

Claims 1 through 50 are currently pending in the application.

Claims 17, 18, 25, 42, and 43 have been withdrawn from consideration as being directed to a non-elected invention.

Claims 1 through 16, 19 through 24, 26 through 41, and 44 through 50 currently stand rejected.

Claims 1, 6, 10, 14, 16, 26, 31, 35, and 39 have been amended.

This amendment is in response to the final Office Action of November 18, 2003.

Information Disclosure Statement(s)

Applicant notes the filing of three Information Disclosure Statements herein on August 29, 2001, August 22, 2002 and October 23, 2003 and notes that copies of the PTO-1449s were not returned with the outstanding Office Action. Applicant respectfully requests that the information cited on the PTO-1449s be made of record herein.

35 U.S.C. § 102(e) Rejections

Anticipation Rejection Based on Estes et al. (U.S. Patent 6,410,415)

Claims 1, 3, 6, 8, 10, 12, 14, 16, 26, 28, 31, 33, 35, 37, 39, 41 were rejected under 35 U.S.C. § 102(e) as being anticipated by Estes et al. (U.S. Patent 6,410,415). Applicant has amended claims 1, 6, 10, 14, 16, 26, 31, 35, and 39 to define over the Estes reference.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

The Estes Patent discloses a semiconductor assembly having an IC chip 1 including an active surface having at least one bond pad 6 and at least one bump 2 attached thereto. The bump 2 connects one bond pad on the active surface of the IC chip 1 to the substrate bond pads 4

on a substrate 3. An electrically insulating adhesive 5 is provided between the substrate 3 and the IC chip 1.

Presently amended independent claims 1, 26, and 31 recite the limitation "a wetting agent layer of about a monolayer thick thereon, said wetting agent layer wetable by a polymeric material." The Estes Patent fails to disclose a wetting agent layer of about a monolayer thick that is wetable by a polymeric material to anticipate the presently claimed invention under 35 U.S.C. § 102.

In contrast, the Estes reference generally discloses an electrically insulating adhesive 5 located between an IC chip 1 and a circuit board (substrate 3). The Estes reference does not disclose a monolayer thick wetting agent layer having the specific wetting properties as recited in presently amended claims 1 and 26. Therefore, presently amended independent claims 1, 26, and 31 and claims depending therefrom are not anticipated by the Estes reference.

Similarly, presently amended independent claims 6 and 31 recite the limitation "a wetting agent layer provided on said active surface of said semiconductor, said wetting agent layer having a thickness of about a monolayer and wetable by a polymeric material." As stated above, the Estes reference fails to disclose a monolayer thick wetting agent layer having the specific wetting properties recited in the presently amended independent claims 6 and 31. Therefore, presently amended independent claims 6 and 31 and claims depending therefrom are not anticipated by the Estes reference.

Presently amended independent claims 10 recites the limitations of "a wetting agent located on a portion of said active surface of said semiconductor device; and
an underfill material substantially filling a volume located between said substrate and said wetting agent." Similarly, presently amended independent claim 14 recites the limitations of "a wetting agent layer provided on at least a portion of said active surface of said semiconductor device, the underfill material substantially filling a volume between the wetting agent layer and said upper surface of said substrate."

The Estes reference fails to disclose a wetting agent or wetting agent layer located on a portion of the active surface of IC chip 1 and an underfill material filling a volume between the wetting agent or wetting agent layer and the substrate 3. The Estes reference merely discloses

electrically insulating adhesive 5 disposed between the IC chip 1 and the substrate 3. The Estes reference does not disclose an intervening wetting agent or wetting agent layer between electrically insulating adhesive 5 and IC chip 1. Therefore, presently amended independent claims 10 and 14 and claims depending therefrom are not anticipated by the Estes reference.

Presently amended independent claim 35 recites the limitations "a wetting agent located on a portion of said active surface of said semiconductor die; and an underfill material located between said substrate and said semiconductor die." Presently amended independent claim 39 recites the limitations of an underfill material provided between said substrate and said semiconductor die; and a wetting agent layer provided on at least a portion of said active surface of said semiconductor die."

The Estes reference fails to disclose a wetting agent or a wetting agent layer located on a portion of the active surface of its IC chip 1 and an underfill material disposed between its IC chip 1 and substrate 3. In contrast, the Estes reference discloses electrically insulating adhesive 5 filling the space between the IC chip 1 and substrate 3. Therefore, presently amended independent claims 35 and 39 and claims depending therefrom are not anticipated by the Estes reference.

35 U.S.C. § 103(a) Rejections

Obviousness Rejection Based on Estes et al. (U.S. Patent 6,410,415) in view of Wong et al. (U.S. Patent 6,180,696)

Claims 2, 4, 5, 7, 9, 11, 13, 15, 19, 27, 29, 30, 32, 34, 36, 38, 40 and 44 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Estes et al. (U.S. Patent 6,410,415) in view of Wong et al. (U.S. Patent 6,180,696). Applicant respectfully traverses this rejection, as hereinafter set forth.

Applicant further submits that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or

suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure.

Claims 2, 4, 5, 7, 9, 11, 13, 15, 19, 27, 29, 30, 32, 34, 36, 38, 40, and 44 are nonobvious for at least depending from a patentable independent claim as stated above in the section regarding the Estes reference.

Obviousness Rejection Based on Estes et al. (U.S. Patent 6,410,415) in view of DeFelice et al. (U.S. Patent 6,190,940)

Claims 20, 21, 23, 24, 45, 46, 48 and 49 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Estes et al. (U.S. Patent 6,410,415) in view of DeFelice et al. (U.S. Patent 6,190,940). Applicant respectfully traverses this rejection, as hereinafter set forth.

The Estes reference teaches or suggests a semiconductor assembly having an IC chip 1 including an active surface having at least one bond pad 6 and at least one bump 2 attached thereto. The bump 2 connects one bond pad on the active surface of the IC chip 1 to the substrate bond pads 4 on a substrate 3. An electrically insulating adhesive 5 is provided between the substrate 3 and the IC chip 1.

The DeFelice Patent teaches or suggests an IC chip 21 with solder bump sites 22 and solder bumps 41. The active surface of the IC chip 21 is coated with an epoxy layer 23. An interconnection substrate 37 having bonding sites 38 is coated with a layer of epoxy 39 to ensure wetting of the substrate with epoxy. The solder bumps 41 of the IC chip 21 are interconnected with the bonding sites 38 of the interconnection substrate 37 by urging them together, the solder bumps 41 penetrating the layer of epoxy 39 coating the bonding sites 38.

Independent claims 20, 23, 45, and 48 require that a wetting agent or wetting agent layer be provided on both a portion of the active surface and a portion of the upper surface of the substrate. Neither, the Estes nor the DeFelice Patent teaches or suggests a wetting agent or wetting agent layer provided on a portion of the active surface.

There is no motivation or suggestion in the cited art to modify the disclosure of the Estes reference by adding a wetting layer as in the DeFelice reference. There is no reason to provide a

wetting agent between the electrically insulating adhesive 5 and the substrate 3 of the Estes reference. In fact, the Estes reference teaches away from providing such a layer because electrically insulating adhesive 5 is applied directly to the substrate 3. Furthermore, there is no reason to provide a wetting agent on the active surface of the IC chip 1 of the Estes reference. It is not necessary or desirable to add a wetting agent to the semiconductor package of the Estes reference because the electrically insulating adhesive 5 is not formed by underfilling a semiconductor assembly of an IC chip 1 and a substrate 3. In contrast, the electrically insulating adhesive 5 is preformed on the substrate 3 and then the IC chip 1 is pressed on the substrate 3 to make electrical contact therebetween. Wetting of the electrically insulating adhesive 5 to IC chip or the substrate 3 is not a concern or problem recognized by the Estes reference because the semiconductor package is not formed by underfilling, but by way of application of the electrically insulating adhesive 5 to substrate 3 followed by pressing the IC chip 1 onto the substrate 3 to bond thereto.

Furthermore, although the DeFelice reference teaches or suggests a layer of epoxy 39 to ensure wetting of the substrate with epoxy, it does not teach or suggest providing another layer of epoxy 39 on the active surface of IC chip 21. The combination of the Estes reference and the DeFelice reference fails to recognize the problem with having an underfill material wet the surface of a semiconductor substrate. In fact, the DeFelice reference teaches away from using an additional layer of epoxy 39 on the active surface of a chip by illustrating the epoxy layer 23 bonded directly to the active surface of IC chip 21. This illustrates that the DeFelice reference does not recognize that there would be a problem with the epoxy layer 23 wetting the active surface of the IC chip 21. The Estes reference also fails to provide such a teaching. Only by using impermissible hindsight would a wetting layer be added to the active surface of IC chip 1 of the Estes reference. The Office Action has not provided a rationale from the cited art to modify the Estes reference by adding a wetting layer. Therefore, independent claims 20, 23, 45, and 48 and claims depending therefrom are nonobvious in view of the Estes reference and the DeFelice reference.

Obviousness Rejection Based on Estes et al. (U.S. Patent 6,410,415) and DeFelice et al. (U.S. Patent 6,190,940) as applied to claims 20 and 45 above, and further in view of Wong et al. (U.S. Patent 6,180,696)

Claims 22 and 47 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Estes et al. (U.S. Patent 6,410,415) and DeFelice et al. (U.S. Patent 6,190,940) as applied to claims 20 and 45 above, and further in view of Wong et al. (U.S. Patent 6,180,696). Applicant respectfully traverses this rejection, as hereinafter set forth.

Claims 22 and 47 are nonobvious for at least depending from patentable independent claims 20 and 45 as stated above in the section regarding rejection of claims 20 and 45.

CONCLUSION

Applicant submits that claims 1 through 50 are clearly allowable over the cited prior art. Applicant requests the allowance of claims 1 through 50 and the case passed for issue.

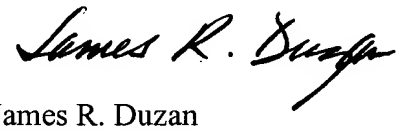
The Applicant requests entry of this amendment for the following reasons.

The claims as amended avoid the rejection set forth in the office action;

No new matter is presented in the amendments; and

The amendment is timely filed.

Respectfully submitted,



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